2018: The Year Certifiable Multicore Takes Off

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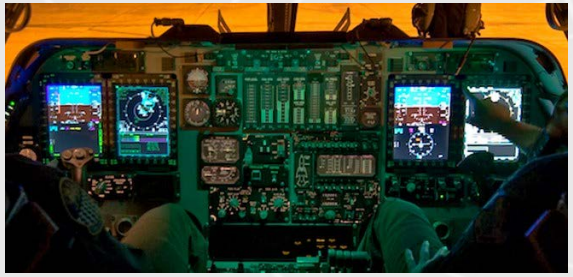
A Brief History of Avionics processing

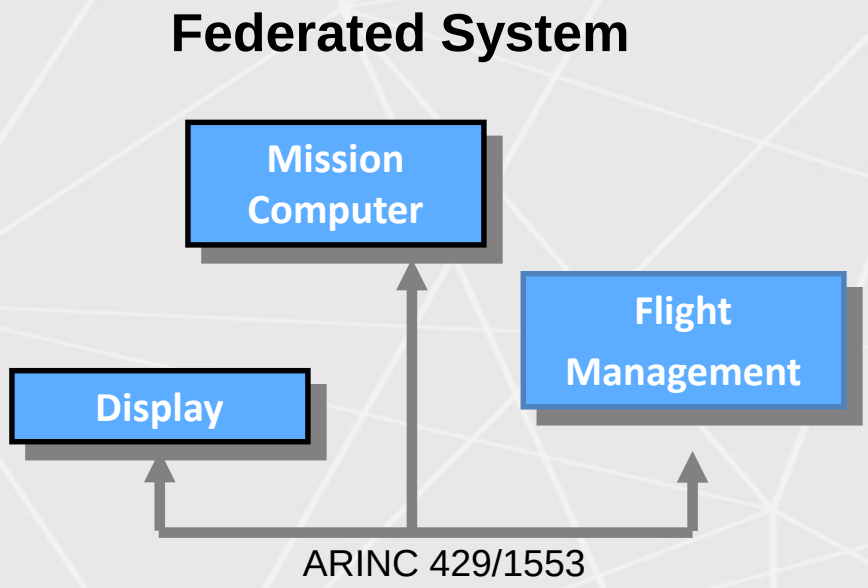
Analog Systems

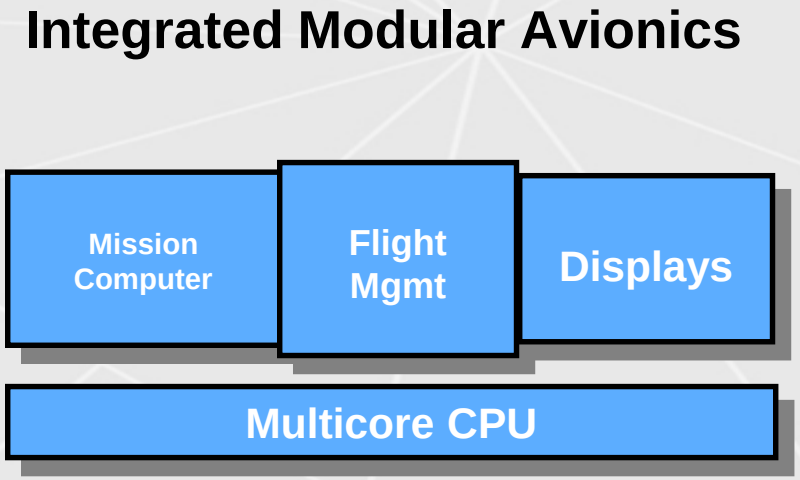
Federated



Future

A Brief History of Avionics processing





A Brief History of Avionics processing

- Federated Systems (single functions boxes distributed through the aircraft)
- Integrated Module Avionics (mainly in commercial where a complete new airframe/avionics system could be designed from the ground up)
- Future of Avionics, Information and knowledge centric possibly deploying AI/Deep Learning Neural Networks
  - New trend that A&D will learn from other markets. Advancements in Auto, robotics, AI will be incubated outside of A&D.

Many of the systems we see are stuck between Federated and IMA

- Especially true in DoD programs, there is never an opportunity to completely redesign
- “Integration without adult supervision” – functionality has been added over many years one subsystem at a time without system level redesign
- High cost of certification and recertification encourages the re-use of existing certified components

What does this have to do with Multicore CPUs?

- No longer able to achieve dramatic improvements in CPUs via increased clock speed (from >30% per Moore's Law cycle to ~10%)
- Processor companies aren't interested in new single CPU designs
- Mixed criticality presents many architectural decisions:
  - Homogeneous or heterogeneous cores
  - Multiple Operating Systems
- In order to consolidate functionality into fewer subsystems, multicore is needed
- Ever increasing demand for SWaP reductions

We need to be able to use multicore!

Historical Factors in CPU Selection

- Performance/Power dissipation
- Obsolescence
- Technical Readiness Level (TRL) and/or Certification History
- Availability of design information

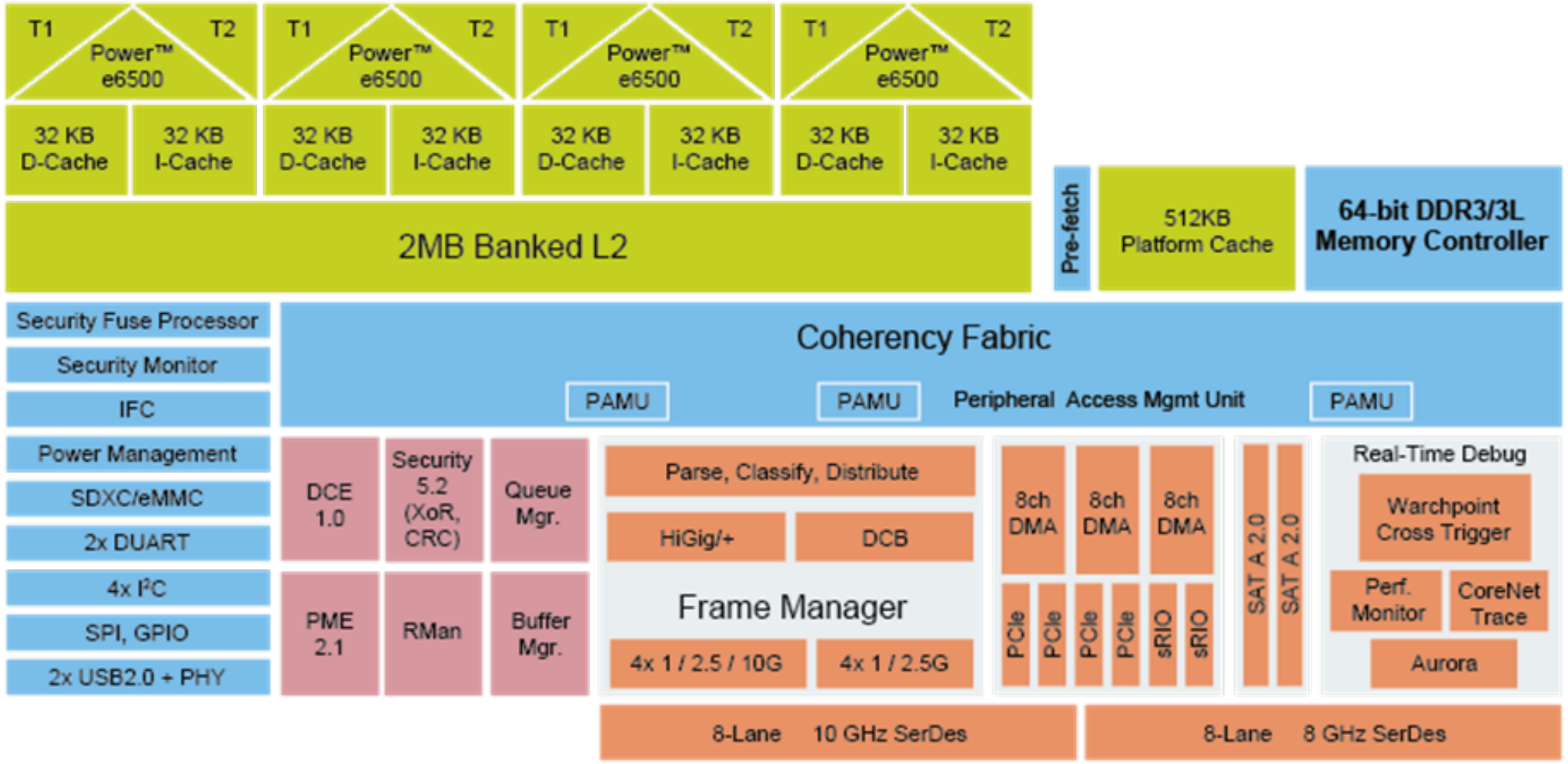
Future Factors in CPU Selection

- Performance/Power dissipation
- Obsolescence
- Technical Readiness Level (TRL) and Certification History
- **Availability of design information**
- **Determinism**
- **Isolation**
- **Software ecosystem**
- **Flexibility of architectural choices**
- **Uncertainty of the future of Safety Silicon, which architecture will replace PPC**

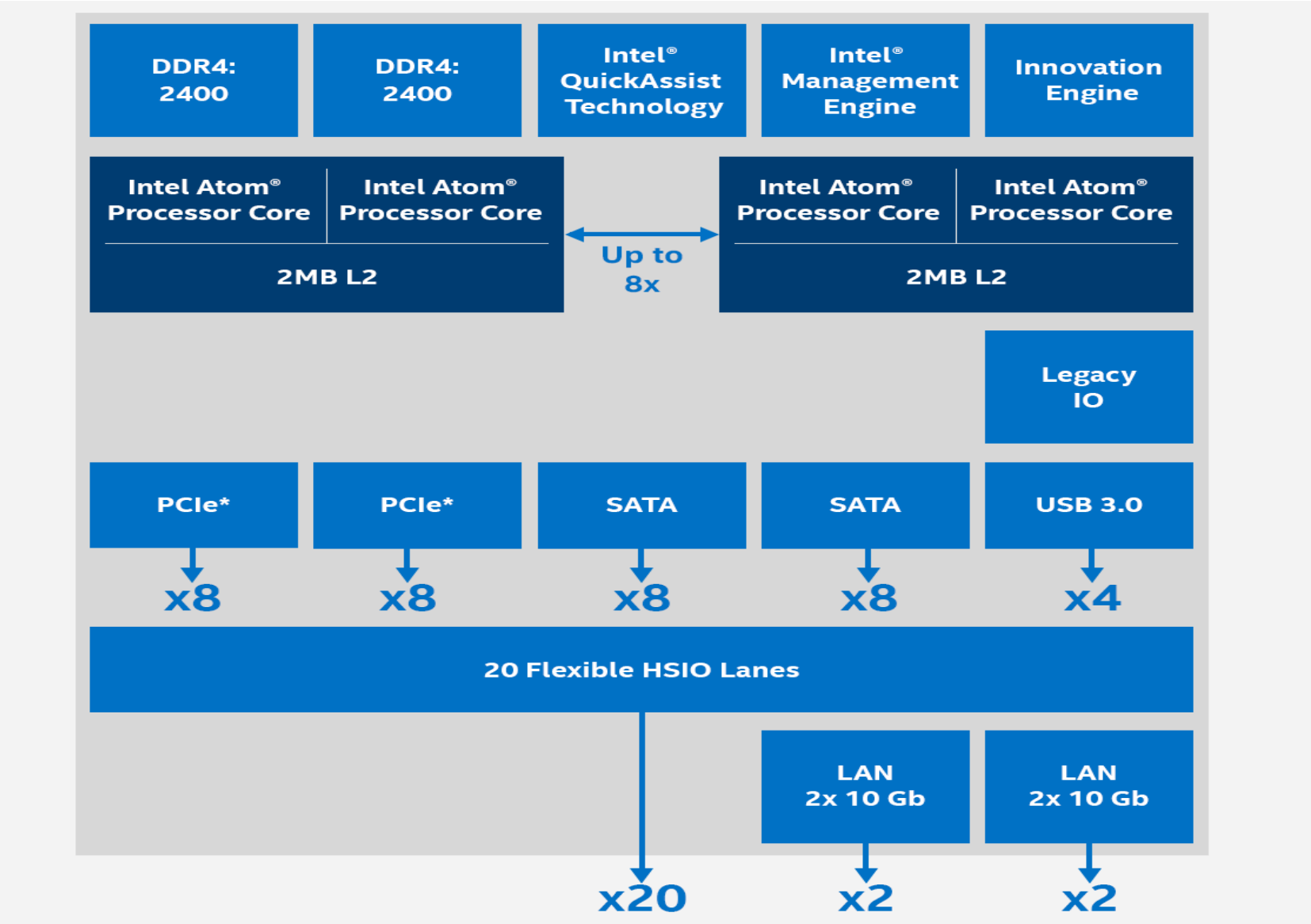
Problems unique to avionics

- System lifecycles over 20+ years
- Certification requirements
- Determinism
- Isolation
- Cost and time of certification/recertification
- Certification artifacts needed on all of the components
- Security. In a multicore CPU how to ensure applications data is kept private and how do you control the flow of information

The root of the problem: T2080



The root of the problem: Intel Atom



The root of the problem

- Shared Resources
  - Always there is some level of shared resources, single memory controllers, shared CPU bus, cache. Byproduct of using CPUs designed for the enterprise customer.
- The use of shared resources causes interference
- The amount of interference increases with the number of cores used
- Interference is application dependent and use-case unique. Unlikely that every interference can be mitigated for every use-case.
  - May limit some of the architectural options, especially early on

All the pieces are coming together….

- Certification authorities are further along in their understanding of multicore and their guidelines are becoming more prescriptive.
  - Introduction of CAST32
  - Newer CAST32A
  - Evolving ARINC 653 standard
  - MCFA (Multicore for Avionics) Industry Working Group
- Interference is becoming more and more understood, especially by the software companies
- Hardware and software companies are sharing information
- Simple multicore designs going through certification

There is less uncertainty surrounding multicore

Platform provider and System Integrators are big jobs that require close collaboration

- DO-297 Role Separation: Stakeholders defined as Platform Supplier, System Integrator and Application Suppliers
- IMA is pushing everyone to think in terms of Systems
- Platform Provider must work closely with software ecosystem to provide a platform in which interference is understood and minimized. Interference that cannot be eliminated is mitigated
- Greater number of requirements and constraints levied on the Application Suppliers relating to integration with the system
- Tighter partnerships between hardware and software companies
- The huge number of potential architectural decisions may influence CPU selection

Multicore Certification is a team effort

Summary

- Industry's understanding and 'comfort' of multicore is increasing
- There are some certifications already underway;
  we will be learning a lot as these progress
- Vast number of architectural (HW and SW) choices and use-cases
- Tighter collaboration with vendors is a must
- Tighter collaboration between Platform Provider and Customer will ease certification effort

Multicore Certification is going to happen!

Thank You!

Questions?